Below are 18 review problems to help you prepare for our 2nd exam. If you do all the problems prior to class on Monday, you will earn 4 points extra credit. Go for it! NOTE: the exam will also have true/false, fill in the blank, and multiple choice questions. You would be wise to study all the terminology we have learned in the class for Chapters 3, 5, 6, and 7.

1. List the five process states discussed in class (include exit) and define each with one sentence.

2. Define difference between and I/O intensive and a compute intensive process. What does the OS do to ensure a compute intensive process does not “hog” the system?

3. Suppose the overhead to swap a running process with a ready process is 1 ms. Would a time slice of 1 ms be a good time slice amount?

4. How long would it take to transmit a 10MB file using each of the following media. Assume 1 Kbps = 1024 bps, etc.
   a. A 56 Kbps modem (dial up)
   b. A 1.5 Mbps DSL line (an older DSL line)
   c. A 100 Mbps Ethernet link (Fast Ethernet)

5. Name the layers in the Internet Protocol Stack and describe the goal of each layer.
6. The figure below shows two shared bus networks connected via a bridge.
   a. If A is transmitting a packet to B, will D look at the packet and ask “is this for me”?
   b. If A is transmitting a packet to C, will D look at the packet and ask “is this for me”?
   c. Would your answers to a or b change if the bridge was a repeater instead? Explain.
   d. Would your answers to a or b change if the network was a star with a central switch connected to all nodes (see figure above)? Explain.

7. Suppose node A is sending node B a packet using the ARQ algorithm.
   a. Suppose packet 4 is lost from A to B. Which node(s) respond and how?
   b. Suppose the ACK for packet 7 is lost from B to A. Which node(s) respond and how?

8. Consider the network shown below with the current measured delays between two nodes.
   a. List all possible simple paths between nodes A and D; simple paths are those that do not repeat a node (i.e., no loop).
   b. Which path provides the shortest delay?
9. Assume when accessing data in cache, a hit takes 0.5 ns and happens 90% of the time, and a miss takes 10 ns.
   a. What is the average time spent on hits?
   b. What is the average time spent on misses?

10. A CPU accesses 250 program instructions. Each memory access takes 5 ns. The memory can only hold 50 instructions. The first 50 instructions are already in memory. Replacing 50 instructions with the next 50 instructions takes 400 ns. What is the total time?

11. What are the four sub-systems of a computer? Describe the purpose for each.

12. What is the difference between Memory Address Register and Memory Data Register?

13. Assume the time to access RAM is 50 ns and the access time for cache is 5 ns. The cache miss rate is 5%. What is the overall average access time?

14. How can a system designer increase cache hit ratio?

15. Describe two key issues with von Neumann architectures, and how they might be resolved.
16. Assume the following instruction set
   000 STOP
   001 ADD
   010 SUB
   011 INPUT
   100 OUTPUT
   101 JUMP
   110 UNUSED
   111 UNUSED

   Assume the following instruction format

<table>
<thead>
<tr>
<th>Opcode (3 bits)</th>
<th>Address Field (4 bits)</th>
<th>Address Field (4 bits)</th>
<th>Address Field (4 bits)</th>
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   Input x to M[12]
   Input y to location M[14]
   Input z to location M[9]
   z = x + y
   y = x − z
   Output z to location M[13]

17. If an opcode is 3 bits - how many instructions in the instruction set?

18. If the address field is 4 bits what is the size of memory?